Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

1. (Previously Presented) A method of manufacturing an insulated gate semiconductor device, said method comprising:

forming a resist over a crystal semiconductor comprising a part to become a channel forming region;

forming a dotted hole in said resist by patterning said resist using electron drawing method or FIB method;

forming an intrinsic or substantially intrinsic region and impurity regions in said part to become the channel forming region by introducing a first impurity into said channel forming region through said resist having said dotted hole, said first impurity being selected from the group consisting of carbon, nitrogen and oxygen; and

introducing into said crystal semiconductor a second impurity that gives one conductivity to form a source region and a drain region in said crystal semiconductor with said channel forming region therebetween,

wherein said impurity regions have total width of Wpi in a direction of a channel width W, and a total width of said intrinsic or substantially intrinsic region is Wpa in said direction of said channel width W, where Wpi/W = 0.1 to 0.9 and Wpa/W = 0.1 to 0.9, and

wherein said source region and said drain region and said channel forming region are provided in a transistor of at least one selected from the group consisting of an arithmetic operating section, a memory section, a DRAM circuit and an SRAM circuit.

2. (Original) A method as claimed in claim 1 further comprising the steps of:

forming a gate insulating film over said part to become the channel forming region after the step of forming said plurality of impurity regions; and

forming a gate electrode over said part to become the channel forming region with said gate insulating film therebetween.

3. (Previously presented) A method of manufacturing an insulated gate semiconductor device, said method comprising the steps of:

locally conducting an anisotropic etching on a surface of a substrate comprising silicon to draw a groove-like or hole-like pattern in a part of said substrate to become a channel forming region:

adding said surface of said substrate with an impurity selected from the group consisting of carbon, nitrogen and oxygen;

embedding said groove-like or hole-like pattern with thermal oxide by conducting a heat treatment on said substrate after the adding step to make said impurity segregated in said thermal oxide.

4. (Original) A method as claimed in claim 3 wherein said heat treatment is conducted at a temperature of 1000 to 1200 °C.

5. (Previously presented) A method of manufacturing an insulated gate semiconductor device, said method comprising the steps of:

locally conducting an anisotropic etching on a surface of a substrate comprising silicon and containing boron to draw a groove-like or hole-like pattern in a part of said substrate to become a channel forming region;

adding said surface of said substrate with an impurity selected from the group consisting of carbon, nitrogen and oxygen;

embedding said groove-like or hole-like pattern with thermal oxide by conducting a heat treatment on said substrate after the adding step to make said impurity segregated in said thermal oxide and to make said boron segregated in said thermal oxide.

6. (Original) A method as claimed in claim 5 wherein said heat treatment is conducted at a temperature of 1000 to 1200 °C.

7. (Previously presented) A method of manufacturing an insulated gate semiconductor device, said method comprising:

implanting an oxygen ion into a crystal semiconductor comprising a part to become a channel forming region by a convergent ion beam or an electron beam, said crystal semiconductor comprising silicon;

forming an intrinsic or substantially intrinsic region and oxide regions in said part to become the channel forming region by thermally treating said crystal semiconductor comprising silicon at a temperature of 1000 °C or higher to change a region regions of said crystal semiconductor implanted with said oxygen ion by said implanting step into said oxide regions; and

introducing into said crystal semiconductor an impurity that gives one conductivity to form a source region and a drain region in said crystal semiconductor with said channel forming region therebetween, and

wherein said oxide regions form one or a plurality of rows extending in a direction of a channel length of said channel forming region.

8. (Original) A method as claimed in claim 7 further comprising the steps of:

forming a gate insulating film over said part to become the channel forming region after the thermally treating step; and

forming a gate electrode over said part to become the channel forming region with said gate insulating film therebetween.

9. (Previously Presented) A method of manufacturing an insulated gate semiconductor device, said method comprising:

forming an intrinsic or substantially intrinsic region and impurity regions in a part of a crystal semiconductor to become a channel forming region by introducing a first impurity into said channel forming region, said impurity regions containing an element selected from the group consisting of carbon, nitrogen and oxygen as said first impurity; and

introducing into said crystal semiconductor a second impurity that gives one conductivity to form a source region and a drain region in said crystal semiconductor with said channel forming region therebetween,

wherein said impurity regions have total width of Wpi in a direction of a channel width W, and a total width of said intrinsic or substantially intrinsic region is Wpa in said direction of said channel width W, where Wpi/W = 0.1 to 0.9 and Wpa/W = 0.1 to 0.9, and

wherein said impurity regions form one or a plurality of rows extending in a direction of a channel length of said channel forming region.

10. (Original) A method as claimed in claim 9 further comprising the steps of:

forming a gate insulating film over said part to become the channel forming region after the step of introducing the first impurity; and

forming a gate electrode over said part to become the channel forming region with said gate insulating film therebetween.

11. (Previously presented) A method of manufacturing an insulated gate semiconductor device, said method comprising the steps of:

locally conducting an anisotropic etching on a surface of a substrate comprising silicon to draw a groove-like or hole-like pattern in a part of said substrate to become a channel forming region;

adding said surface of said substrate with an impurity selected from the group consisting of carbon, nitrogen and oxygen;

embedding said groove-like or hole-like pattern with thermal oxide by conducting a heat treatment on said substrate after the adding step to make said impurity segregated in said thermal oxide,

wherein said impurity is added by said adding step to said substrate to a depth deeper than an etched depth formed in said groove-like or hole-like pattern by said anisotropic etching.

12. (Original) A method as claimed in claim 11 wherein said heat treatment is conducted at a temperature of 1000 to 1200 °C.

13. (Previously Presented) A method of manufacturing an insulated gate semiconductor device, said method comprising the steps of:

forming an intrinsic or substantially intrinsic region and a plurality of impurity regions in a part of a crystal semiconductor to become a channel forming region by introducing a first impurity into said impurity regions, said plurality of impurity regions containing an element selected from the group consisting of carbon, nitrogen and oxygen as said first impurity;

introducing into said crystal semiconductor a second impurity that gives one conductivity to form a source region and a drain region in said crystal semiconductor with said channel forming region therebetween,

wherein said impurity regions alternate with said intrinsic or substantially intrinsic region in a direction of a channel width W of said channel forming region, and

wherein said impurity regions have total width of Wpi in a direction of said channel width W, and a total width of said intrinsic or substantially intrinsic region is Wpa in said direction of said channel width W, where Wpi/W = 0.1 to 0.9 and Wpa/W = 0.1 to 0.9, and

wherein said impurity regions form one or a plurality of rows extending in a direction of a channel length of said channel forming region.

14. (Original) A method as claimed in claim 13 further comprising the steps of:

forming a gate insulating film over said part to become the channel forming region after the step of introducing the first impurity; and

forming a gate electrode over said part to become the channel forming region with said gate insulating film therebetween.

15. (Previously presented) A method of manufacturing an insulated gate semiconductor device, said method comprising:

forming a resist over a crystal semiconductor comprising a part to become a channel forming region;

forming a dotted hole in said resist by patterning said resist using electron drawing method or FIB method;

forming an intrinsic or substantially intrinsic region and a plurality of impurity regions in said part to become the channel forming region by introducing a first impurity into said impurity regions through said resist having said dotted hole, said first impurity being selected from the group consisting of carbon, nitrogen and oxygen; and

introducing into said crystal semiconductor a second impurity that gives one conductivity to form a source region and a drain region in said crystal semiconductor with said channel forming region therebetween,

wherein said impurity regions form one or a plurality of rows extending in a direction of a channel length of said channel forming region, and

wherein said impurity regions have total width of Wpi in a direction of a channel width W, and a total width of said intrinsic or substantially intrinsic region is Wpa in said direction of said channel width W, where Wpi/W = 0.1 to 0.9 and Wpa/W = 0.1 to 0.9.

16. (Original) A method as claimed in claim 15 further comprising the steps of:

forming a gate insulating film over said part to become the channel forming region after the step of forming said plurality of impurity regions; and

forming a gate electrode over said part to become the channel forming region with said gate insulating film therebetween.

17. (Previously presented) A method of manufacturing an insulated gate semiconductor device, said method comprising the steps of:

locally conducting an anisotropic etching on a surface of a substrate comprising silicon to draw a groove-like or hole-like pattern in a part of said substrate to become a channel forming region;

adding said surface of said substrate with an impurity selected from the group consisting of carbon, nitrogen and oxygen;

embedding said groove-like or hole-like pattern with thermal oxide by conducting a heat treatment on said substrate after the adding step to make said impurity segregated in said thermal oxide,

wherein said impurity segregated in said thermal oxide forms a plurality of impurity regions

wherein said impurity regions form one or a plurality of rows extending in a direction of a channel length of said channel forming region.

18. (Previously presented) A method of manufacturing an insulated gate semiconductor device, said method comprising the steps of:

forming a source region, a drain region and a channel forming region using a crystal semiconductor;

forming an intrinsic or substantially intrinsic region and impurity regions in said channel forming region; and

forming a gate insulating film and a gate electrode over said channel forming region,

wherein said impurity regions formed in said channel forming region pins a depletion layer that expands from said drain region toward said channel forming region and said source region, and

wherein a carrier moves through said intrinsic or substantially intrinsic region while said carrier avoids said impurity region formed in said channel forming region, and

wherein said impurity regions form one or a plurality of rows extending in a direction of a channel length of said channel forming region.

19. (Previously presented) A method of manufacturing an insulated gate semiconductor device, said method comprising the steps of:

forming a source region, a drain region and a channel forming region using a crystal semiconductor;

forming an intrinsic or substantially intrinsic region and impurity regions in said channel forming region;

forming a gate insulating film and a gate electrode over said channel forming region,

wherein said impurity regions control the threshold voltage to a predetermined value voltage, and

wherein a carrier moves through said intrinsic or substantially intrinsic region while said carrier avoids said impurity regions formed in said channel forming region, and

wherein said impurity regions form one or a plurality of rows extending in a direction of a channel length of said channel forming region.

20. (Previously presented) A method of manufacturing an insulated gate semiconductor device, said method comprising:

forming a source region, a drain region and a channel forming region using a crystal semiconductor;

adding impurity elements that expand an energy band width (Eg) to said channel forming region to form an intrinsic or substantially intrinsic region and an impurity regions in said channel forming region; and

forming a gate insulating film and a gate electrode over said channel forming region,

wherein said impurity regions have total width of Wpi in a direction of a channel width W, and a total width of said intrinsic or substantially intrinsic region is Wpa in said direction of said channel width W, where Wpi/W = 0.1 to 0.9 and Wpa/W = 0.1 to 0.9, and

wherein said impurity regions form one or a plurality of rows extending in a direction of a channel length of said channel forming region.

21. (Previously Presented) A method of manufacturing an insulated gate semiconductor device, said method comprising the steps of:

forming a source region, a drain region and a channel forming region using a crystal semiconductor;

adding impurity elements that expand an energy band width (Eg) to said channel forming region to form an intrinsic or substantially intrinsic region and impurity regions in said channel forming region; and

forming a gate insulating film and a gate electrode over said channel forming region,

wherein said impurity regions pin a depletion layer that expands from said drain region toward said channel forming region and said source region,

wherein a carrier moves through said intrinsic or substantially intrinsic region while said carrier avoids said impurity regions formed in said channel forming region, and

wherein said impurity regions form one or a plurality of rows extending in a direction of a channel length of said channel forming region.

22. (Previously presented) A method of manufacturing an insulated gate semiconductor device, said method comprising the steps of:

forming a source region, a drain region and a channel forming region using a crystal semiconductor;

adding impurity elements that expand an energy band width (Eg) to said channel forming region to form an intrinsic or substantially intrinsic region and impurity regions in said channel forming region; and

forming a gate insulating film and a gate electrode over said channel forming region,

wherein said impurity regions control the threshold voltage to a predetermined value voltage,

wherein an impurity element that expand an energy band width (Eg) is added to said impurity region, and

wherein a carrier moves through said intrinsic or substantially intrinsic region while said carrier avoids said impurity regions formed in said channel forming region, and

wherein said impurity regions form one or a plurality of rows extending in a direction of a channel length of said channel forming region.

23. (Previously presented) A method of manufacturing an insulated gate semiconductor device, said method comprising:

forming a source region, a drain region and a channel forming region using a crystal semiconductor; and

adding impurity elements that expand an energy band width (Eg) to said channel forming region to form an intrinsic or substantially intrinsic region and an impurity regions in said channel forming region; and

forming a gate insulating film and a gate electrode over said channel forming region,

wherein said impurity region has an insulating property,

wherein an impurity element that expands an energy band width (Eg) is added to said impurity region, and

wherein said impurity regions have total width of Wpi in a direction of a channel width W, and a total width of said intrinsic or substantially intrinsic region is Wpa in said direction of said channel width W, where Wpi/W = 0.1 to 0.9 and Wpa/W = 0.1 to 0.9, and

wherein said impurity regions form one or a plurality of rows extending in a direction of a channel length of said channel forming region.

24. (Cancelled)

25. (Original) A method of manufacturing an insulated gate semiconductor device as claimed in claim 18, wherein assuming that a width of said channel forming region is W, a total width of said impurity regions is Wpi, and a total of intervals of said impurity regions is Wpa, respectively, relational expressions of Wpi/W = 0.1 to 0.9, Wpa/W = 0.1 to 0.9 and Wpi/Wpa = 1/9 to 9 are accomplished between W, Wpi and Wpa.

26. (Original) A method of manufacturing an insulated gate semiconductor device as claimed in claim 18, wherein at least one section perpendicular to a channel direction of said channel forming region is substantially regarded as an assembly of a plurality of channel forming regions which are sectioned by said impurity regions.

27. (Original) A method of manufacturing an insulated gate semiconductor device as claimed in claim 18, wherein said impurity regions are arranged at intervals of 100 to 3000 Å.

28. (Original) A method of manufacturing an insulated gate semiconductor device as claimed in claim 18, wherein said crystal semiconductor is a monocrystal semiconductor.

29. (Original) A method of manufacturing an insulated gate semiconductor device as claimed in claim 18, wherein said impurity regions are in a dot pattern.

30. (Cancelled)

31. (Original) A method as claimed in claim 19, wherein assuming that a width of said channel forming region is W, a total width of said impurity regions is Wpi, and a total of intervals of said impurity regions is Wpa, respectively, relational expressions of Wpi/W = 0.1 to 0.9, Wpa/W = 0.1 to 0.9 and Wpi/Wpa = 1/9 to 9 are accomplished between W, Wpi and Wpa.

32. (Original) A method as claimed in claim 19, wherein at least one section perpendicular to a channel direction of said channel forming region is substantially regarded as an assembly of a plurality of channel forming regions which are sectioned by said impurity regions.

33. (Original) A method as claimed in claim 19, wherein said impurity regions are arranged at intervals of 100 to 3000 Å.

34. (Original) A method as claimed in claim 19, wherein said crystal semiconductor is a monocrystal semiconductor.

35. (Original) A method as claimed in claim 19, wherein said impurity regions are in a dot pattern.

36. (Previously presented) A method as claimed in claim 19, wherein impurity elements for forming said impurity regions are one or a plurality of kinds of elements selected from carbon, nitrogen and oxygen.

37. (Cancelled)

38. (Original) A method as claimed in claim 20, wherein assuming that a width of said channel forming region is W, a total width of said impurity regions is Wpi, and a total of intervals of said impurity regions is Wpa, respectively, relational expressions of Wpi/W = 0.1 to 0.9, Wpa/W = 0.1 to 0.9 and Wpi/Wpa = 1/9 to 9 are accomplished between W, Wpi and Wpa.

39. (Original) A method as claimed in claim 20, wherein at least one section perpendicular to a channel direction of said channel forming region is substantially regarded as an assembly of a plurality of channel forming regions which are sectioned by said impurity regions.

40. (Original) A method as claimed in claim 20, wherein said impurity regions are arranged at intervals of 100 to 3000 Å.

41. (Original) A method as claimed in claim 20, wherein said crystal semiconductor is a monocrystal semiconductor.

42. (Original) A method as claimed in claim 20, wherein said impurity regions are in a dot pattern.

43. (Previously Presented) A method as claimed in claim 20, wherein said impurity elements are one or a plurality of kinds of elements selected from carbon, nitrogen and oxygen.

44. (Cancelled)

45. (Original) A method as claimed in claim 21, wherein assuming that a width of said channel forming region is W, a total width of said impurity regions is Wpi, and a total of intervals of said impurity regions is Wpa, respectively, relational expressions of Wpi/W = 0.1 to 0.9, Wpa/W = 0.1 to 0.9 and Wpi/Wpa = 1/9 to 9 are accomplished between W, Wpi and Wpa.

46. (Original) A method as claimed in claim 21, wherein at least one section perpendicular to a channel direction of said channel forming region is substantially regarded as an assembly of a plurality of channel forming regions which are sectioned by said impurity regions.

47. (Original) A method as claimed in claim 21, wherein said impurity regions are arranged at intervals of 100 to 3000 Å.

48. (Original) A method as claimed in claim 21, wherein said crystal semiconductor is a monocrystal semiconductor.

49. (Original) A method as claimed in claim 21, wherein said impurity regions are in a dot pattern.

50. (Previously Presented) A method as claimed in claim 21, wherein said impurity elements are one or a plurality of kinds of elements selected from carbon, nitrogen and oxygen.

51. (Original) A method as claimed in claim 22, wherein a region other than said impurity regions within said channel forming region is an intrinsic or substantially intrinsic region.

52. (Original) A method as claimed in claim 22, wherein assuming that a width of said channel forming region is W, a total width of said impurity regions is Wpi, and a total of intervals of said impurity regions is Wpa, respectively, relational expressions of Wpi/W = 0.1 to 0.9, Wpa/W = 0.1 to 0.9 and Wpi/Wpa = 1/9 to 9 are accomplished between W, Wpi and Wpa.

53. (Original) A method as claimed in claim 22, wherein at least one section perpendicular to a channel direction of said channel forming region is substantially regarded as an assembly of a plurality of channel forming regions which are sectioned by said impurity regions.

54. (Original) A method as claimed in claim 22, wherein said impurity regions are arranged at intervals of 100 to 3000 Å.

55. (Original) A method as claimed in claim 22, wherein said crystal semiconductor is a monocrystal semiconductor.

56. (Original) A method as claimed in claim 22, wherein said impurity regions are in a dot pattern.

57. (Previously Presented) A method as claimed in claim 22, wherein said impurity elements are one or a plurality of kinds of elements selected from carbon, nitrogen and oxygen.

58. (Cancelled)

59. (Original) A method as claimed in claim 23, wherein assuming that a width of said channel forming region is W, a total width of said impurity regions is Wpi, and a total of intervals of said impurity regions is Wpa, respectively, relational expressions of Wpi/W = 0.1 to 0.9, Wpa/W = 0.1 to 0.9 and Wpi/Wpa = 1/9 to 9 are accomplished between W, Wpi and Wpa.

60. (Original) A method as claimed in claim 23, wherein at least one section perpendicular to a channel direction of said channel forming region is substantially regarded as an assembly of a plurality of channel forming regions which are sectioned by said impurity regions.

61. (Original) A method as claimed in claim 23, wherein said impurity regions are arranged at intervals of 100 to 3000 Å.

62. (Original) A method as claimed in claim 23, wherein said crystal semiconductor is a monocrystal semiconductor.

63. (Original) A method as claimed in claim 23, wherein said impurity regions are in a dot pattern.

64. (Previously Presented) A method as claimed in claim 23, wherein said impurity elements are one or a plurality of kinds of elements selected from carbon, nitrogen and oxygen.

65. (Original) A method as claimed in claim 17 wherein said heat treatment is conducted at a temperature of 1000 to 1200 °C.

66. (Previously presented) A method of manufacturing an insulated gate semiconductor device, said method comprising the steps of:

locally conducting an anisotropic etching on a surface of a substrate comprising silicon and containing boron to draw a groove-like or hole-like pattern in a part of said substrate to become a channel forming region;

adding said surface of said substrate with an impurity selected from the group consisting of carbon, nitrogen and oxygen;

embedding said groove-like or hole-like pattern with thermal oxide by conducting a heat treatment on said substrate after the adding step to make said impurity segregated in said thermal oxide and to make said boron segregated in said thermal oxide,

wherein said impurity segregated in said thermal oxide forms a plurality of impurity regions

wherein said impurity regions form one or a plurality of rows extending in a direction of a channel length of said channel forming region.

67. (Previously presented) A method as claimed in claim 66 wherein said heat treatment is conducted at a temperature of 1000 to 1200 °C.

68. (Previously presented) A method according to claim 1 wherein said intrinsic or substantially intrinsic region contains phosphorus or boron, and concentration of phosphorus or boron therein is $5 \times 10^{17}$ atoms/cm$^3$ or less, and said intrinsic or substantially intrinsic region

contains carbon, nitrogen or oxygen, and concentration of carbon, nitrogen or oxygen therein is 2 x $10^{18}$ atoms/$cm^3$ or less.

69. (Previously presented) A method according to claim 7 wherein said intrinsic or substantially intrinsic region contains phosphorus or boron, and concentration of phosphorus or boron therein is 5 x $10^{17}$ atoms/$cm^3$ or less, and said intrinsic or substantially intrinsic region contains carbon, nitrogen or oxygen, and concentration of carbon, nitrogen or oxygen therein is 2 x $10^{18}$ atoms/$cm^3$ or less.

70. (Previously presented) A method according to claim 9 wherein said intrinsic or substantially intrinsic region contains phosphorus or boron, and concentration of phosphorus or boron therein is 5 x $10^{17}$ atoms/$cm^3$ or less, and said intrinsic or substantially intrinsic region contains carbon, nitrogen or oxygen, and concentration of carbon, nitrogen or oxygen therein is 2 x $10^{18}$ atoms/$cm^3$ or less.

71. (Previously presented) A method according to claim 13 wherein said intrinsic or substantially intrinsic region contains phosphorus or boron, and concentration of phosphorus or boron therein is 5 x $10^{17}$ atoms/$cm^3$ or less, and said intrinsic or substantially intrinsic region contains carbon, nitrogen or oxygen, and concentration of carbon, nitrogen or oxygen therein is 2 x $10^{18}$ atoms/$cm^3$ or less.

72. (Previously presented) A method according to claim 15 wherein said intrinsic or substantially intrinsic region contains phosphorus or boron, and concentration of phosphorus or boron therein is 5 x $10^{17}$ atoms/$cm^3$ or less, and said intrinsic or substantially intrinsic region contains carbon, nitrogen or oxygen, and concentration of carbon, nitrogen or oxygen therein is 2 x $10^{18}$ atoms/$cm^3$ or less.

73. (Previously presented) A method according to claim 18 wherein said intrinsic or substantially intrinsic region contains phosphorus or boron, and concentration of phosphorus or boron therein is $5 \times 10^{17}$ atoms/cm$^3$ or less, and said intrinsic or substantially intrinsic region contains carbon, nitrogen or oxygen, and concentration of carbon, nitrogen or oxygen therein is $2 \times 10^{18}$ atoms/cm$^3$ or less.

74. (Previously Presented) A method of manufacturing an insulated gate semiconductor device, said method comprising:

forming a resist over a crystal semiconductor comprising a part to become a channel forming region;

forming a dotted hole in said resist by patterning said resist using electron drawing method;

forming an intrinsic or substantially intrinsic region and impurity regions in said part to become the channel forming region by introducing a first impurity into said channel forming region through said resist having said dotted hole, said first impurity being selected from the group consisting of carbon, nitrogen and oxygen; and

introducing into said crystal semiconductor a second impurity that gives one conductivity to form a source region and a drain region in said crystal semiconductor with said channel forming region therebetween,

wherein said impurity regions have total width of Wpi in a direction of a channel width W, and a total width of said intrinsic or substantially intrinsic region is Wpa in said direction of said channel width W, where Wpi/W = 0.1 to 0.9 and Wpa/W = 0.1 to 0.9.